<u>**REMARKS**</u>

In this response, claims 67 and 68 have been cancelled, and new claims 71-75 have been added. Accordingly, claims 1-66 and 69-75 are now pending (claims 1, 66, 69, 70, and 75 being independent). The Office Action issued by the Examiner has been carefully considered.

Claims 11, 12 and 15 are amended to correct a self-apparent typographical error. No narrowing of coverage is intended by these amendments.

Claim 68 has been rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Applicant has cancelled claim 68 above without prejudice.

Claims 1-10, 15-18, 21, 25-32, 34-47 and 52-68 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Bowman-Amuah (U.S. Patent No. 6,697,824 B1) in view of Shostack et al. (U.S. Patent No. 6,298,445 B1).

Applicant appreciates the Examiner's response to Applicant's arguments of 15 June 2006. The Examiner makes clear that he presents Shostack to allegedly show first and second processors as claimed in Applicant's independent claim 1. Specifically, the Examiner states that Shostack discloses a real-time update processor 54, and that Shostack discloses a "second processor as the vulnerability database working with the real-time processor."

First, it should be noted that Shostack's vulnerability database is a <u>list</u> of vulnerabilities. As seen in Shostack's Fig. 3, update processor 54 accesses this list from storage device 62, on which the vulnerability database is stored. The accessing of this list does not teach or suggest a second processor as the update processor is the <u>only</u> processor that Shostack describes. The Examiner appears to improperly be attempting to describe a software process executing on update processor 54 as a <u>second</u> processor. However, Shostack describes using a single update

processor 54 to store "an update of a database of security vulnerabilities 92 on a storage device 62" (col. 8, lines 42-54).

Second, even if for the sake of argument Shostack was considered to show two processors, the Examiner respectfully has failed to demonstrate how Shostack teaches or suggests both "performing real-time processes" and any access to the vulnerabilities database as being "other than the real-time processes". Rather, the Examiner describes the processor 54 simply as working with the vulnerabilities database without any argument as to where Shostack teaches both a real-time process and an other than real-time process. There is only the single processor 54, and Shostack does not teach this distinction. Accordingly, Shostack does not teach or suggest a "second processor performing remaining processes other than the real-time processes" as recited by Applicant's claim 1 (emphasis added).

Therefore, the rejection of Applicant's claim 1 should now be withdrawn. Applicant's independent claim 66 is believed allowable for similar reasons.

Applicant appreciates the Examiner's clarifying that Bergkvist is not being relied upon to teach first and second processors. This simplifies the issues in the prosecution of this application.

Applicant's dependent claim 50 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Bowman-Amuah (U.S. Patent No. 6,697,824 B1) and Shostack et al. (U.S. Patent No. 6,298,445 B1) as applied to claim 1 above, and further in view of Vasudevan et al. (U.S. Patent No. 6,715,077 B1).

As discussed in Applicant's prior response, claim 50 recites "establishing a synchronism hierarchy in response to the network resource information". In response, the Examiner states that Vasudevan discloses the support of "various modes of security operation, providing different levels of functionality for the applications 16" (emphasis added). However, Vasudevan only describes providing differing levels of security services to applications (col. 3, lines 36-38).

For example, Vasudevan describes providing different levels of privilege to various applications (col. 3, lines 49-55). Providing security services or differing levels of security privilege does not teach establishing a synchronism hierarchy, and respectfully, the Examiner fails to provide any argument to show a relationship between Vasudevan's teaching and establishing a synchronism hierarchy. Accordingly, Applicant's claim 50 should be allowed.

Claim 69 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Zintel (U.S. Patent No. 6,779,004 B1) in view of Kirby (U.S. Patent No. 6,829,437 B2).

Applicant's independent claim 69 recites a "gateway node comprising a first processor performing real-time processes and a second processor performing high level processing functions." The Examiner cites Zintel as showing such processors at col. 13, lines 38-67. However, Zintel here simply introduces user control points, controlled devices, and bridges as <u>logical</u> nodes on a network. Zintel describes these classifications as referring to functionality rather than physical entities.

Although Zintel describes the packaging of this functionality into physical entities (col. 13, lines 42-46), Zintel does not teach any real-time process distinction between first and second processors as recited by Applicant in claim 69. Further, when Zintel actually does describe the hardware of an exemplary embedded computing device (Figs. 22 and 23), Zintel describes only a <u>single</u> processing unit 902 (col. 45, lines 45-51). Accordingly, this rejection of claim 69 should be withdrawn.

Claim 70 has been rejected under 35 U.S.C. 102(e) as being as anticipated by Zintel (U.S. Patent No. 6,779,004 B1).

Claim 70 as amended recites "establishing a synchronism hierarchy in response to the network timing information". Zintel does not anywhere identically disclose establishing such a synchronism hierarchy <u>as is required for a proper anticipation rejection</u>. The Examiner does

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refer to col. 21, lines 15-55, in an attempt to show a synchronism hierarchy. Yet, here Zintel describes a so-called "rehydrator" 410 that exposes a suitable API to applications. Zintel describes invoking services or responding to events, and specifically teaches a Service Control Protocol Definition. However, this does not disclose establishing a synchronism hierarchy in response to network timing information as Applicant claims.

Claim 70 now further recites "at least one port node configured to receive data from at least one sensor in the vehicle" (emphasis added). Zintel further does not identically describe this. Accordingly, claim 70 should be allowed.

New Claims

New claims 71-75 have been added above. New claims 71-74 depend, directly or indirectly, from independent claim 70 and are believed allowable at least for the reasons discussed above for claim 70.

New independent claim 75 recites "establishing a synchronism hierarchy, being energy usage aware, in response to the network timing information" (emphasis added). Applicant believes that none of the cited art teaches or suggests an energy usage aware synchronism hierarchy established in response to network timing information.
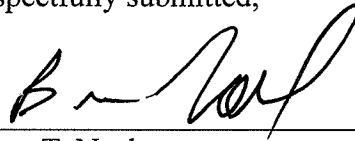
Closing

Applicant's remaining dependent claims not discussed above depend, directly or indirectly, from independent claim 1 and are believed allowable for at least the reasons discussed above for claim 1.

In view of the above, Applicant respectfully requests the reconsideration of this application and the allowance of all pending claims. It is respectfully submitted that the

Examiner's rejections have been successfully traversed and that the application is now in order for allowance. Applicant believes that the Examiner's other arguments not discussed above are moot in light of the above arguments, but reserves the right to later address these arguments. Accordingly, reconsideration of the application and allowance thereof is courteously solicited.

Respectfully submitted,

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